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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/684,988	10/14/2003	Laurent R. Moll	BP3254	4742

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EXAMINER	
NGUYEN, TANH Q	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 06/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/684,988	MOLL, LAURENT R.	
	Examiner	Art Unit	
	Tanh Q. Nguyen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 29-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10, 29-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because The name of the inventor is not in permanent ink, or its equivalent in quality, as required under 37 CFR 1.52(a)(1)(iv). Please note that on the top right corner of page 1 the followings "attorney D cket Number", "First Named Inv ntor", and "Laur nt R. Moll".

Claim Objections

2. Claim 7 is objected to because of the following informalities: Claim 7 recites "selectively disable able" in line 2. It appears that applicant meant to recite "selectively disable".

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

4. Claims 1-10, 29-35 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "the peripheral bus transaction" in lines 6-7, and

"the peripheral bus transaction" in line 11 respectively. There are insufficient antecedent bases for the limitations in the claim. Further it is not clear whether the peripheral bus transactions in line 5 are the same as the peripheral bus transactions in lines 9-10.

Claim 2 recites the limitation "the destination processing device" in line 2. There is insufficient antecedent basis for the limitation in the claim.

Claim 29 recites the limitation " determining an override routing of peripheral bus transactions...based upon a destination node ID of the peripheral bus transaction...". It is not clear how an override routing of (a plurality of) peripheral bus transactions can be based upon information from one peripheral bus transaction,

Claim 30 recites the limitation "the destination processing device" in line 2. There is insufficient antecedent basis for the limitation in the claim.

The rejections that follow are based on the examiner's best interpretation of the claims.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 3, 5, 9, 29, 31, 33, 35 are rejected under 35 U.S.C. 102(b) as being anticipated by Nagami et al. (US 5,835,710).

7. As per claim 1, Nagami teaches a processing device [FIG. 6] comprising:

one or more resources [412, 414 - FIG. 6];

a plurality of peripheral bus interfaces [421, 423, 427 - FIG. 6] operably coupled to the one or more resources and couple able to a peripheral bus fabric [PHYSICAL TRANSMISSION MEDIA, FIG. 6] to support resource sharing with a plurality of other processing devices [601, 602 - FIG. 1];

primary routing resources [FIG. 8; FIG. 10] programmable with a plurality of address ranges [3-5, FIG. 8; VC CONNECTION TARGET IP ADDRESS, FIG. 10], the processing device operable to determine a routing of a peripheral bus transaction among the plurality of peripheral bus interfaces [steps S10-S12, FIG. 7; S167, FIG. 12] based upon a destination address [DESTINATION L3 ADDRESS, FIG. 8; VC CONNECTION TARGET IP ADDRESS, FIG. 10] of the peripheral bus transaction and primary routing resources contents [NEXT HOP L3 ADDRESS, OUTPUT I/F VPI/VCI - FIG. 8; I/F, VPI/VCI, STATUS - FIG. 10]; and

a node ID register [FIG. 8; FIG. 11] programmable with a plurality of override indications [DIRECT for addresses 1-2, FIG. 8; DESTINATION IP ADDRESS, FIG. 11], the processing device operable to determine an override routing of peripheral bus transactions among the plurality of peripheral bus interfaces [steps S9, S12 - FIG. 7; S166, S163 - FIG. 12] based upon a destination node ID [DESTINATION L3 ADDRESS, FIG. 8; DESTINATION IP ADDRESS, FIG. 11] of the peripheral bus transaction and node ID register contents [NEXT HOP L3 ADDRESS, FIG. 8; I/F, VPI/VCI - FIG. 11].

8. As per claim 3, Nagami teaches the processing device ignoring the override routing based upon node ID register contents [for destination addresses 3-5 of FIG. 8, or destination IP address not matching the entry in FIG. 11, override routing is not effected].

9. As per claim 5, Nagami teaches the override routing being applied to I/O peripheral bus transactions [steps S9, S12 - FIG. 7; steps 166-163, FIG. 12].

10. As per claim 9, Nagami teaches the override routing being related to one of the plurality of peripheral bus interfaces and the override routing indicating to route the peripheral bus transaction to either a primary port of the peripheral bus interface or to a secondary port of the peripheral bus interface [FIG. 6].

11. As per claims 29, 33, the claims generally correspond to claim 1, 5 above and are rejected on the same basis.

12. As per claim 31, Nagami teaches routing the peripheral bus transaction according to primary routing base upon node ID register contents [3-5, FIG. 8].

13. As per claim 35, Nagami teaches the primary routing being applied to packet data peripheral bus transactions [steps [S10-S11, FIG. 8; step 167, FIG. 12].

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 2, 4, 6-8, 10; 30, 32, 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagami et al..

16. As per claims 2, 30, Nagami does not teach the node ID of the destination processing device being based upon a set of most significant bits of the destination address of the peripheral bus transaction. Since it was known in the art for a destination address of a transaction over a network to comprise a destination node ID in the most significant bits and other information, and since it was known to use the destination node ID to properly route data through the network, it would have been obvious to one of ordinary skill in the art at the time the invention was made for the destination node ID to be based on the most significant bits of the destination address in order to use the destination node ID to properly route data through the network.

17. As per claims 4, 32, Nagami does not explicitly teach the override routing being applied to cache coherency peripheral bus transactions. Since a cache coherency transaction is an I/O transaction and since applicant did not indicate that it is critical to apply override routing to cache coherency transactions, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply override routing to cache coherency transactions in order to provide alternative paths to the destination.

18. As per claims 6-8, 34, see the rejections of claims 4-5 above. Nagami further teaches the override routing being selectively disable [step 167, FIG. 12], and the override routing not being applied to packet peripheral bus transactions [steps 166, 163 - FIG. 12].

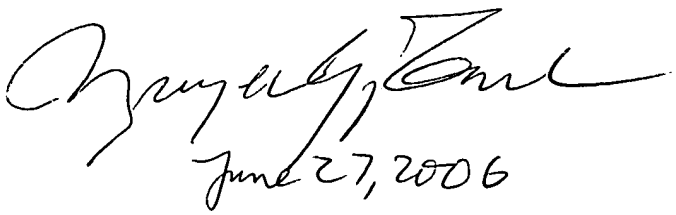
19. As per claim 10, Nagami does not explicitly teaches the elements of each entry in the node ID register. Essentially, Nagami does not teach an override bit and a P/S indication for I/O transactions, and an override bit and P/S indication for cache coherency instructions. Such elements are implementation specific, and It would have been obvious to one of ordinary skill in the art at the time the invention was made to include such elements instead of the effecting the routing algorithm used in Nagami, in order to effect override routing.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tanh Q. Nguyen whose telephone number is 571-272-4154. The examiner can normally be reached on M-F 9:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



TQN
June 27, 2006